SF100/SF600/SF700
In-System Programming (ISP) for SPI NOR Flash

Application Note

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I. Name Interpretation

1. **SPI NOR Flash**: Also known as Serial NOR Flash, BIOS, ROM, Chip, IC.
2. **Programmer**: DediProg's SF100, SF600, SF600*Plus*, SF700.
3. **Chipset**: Include all the application controllers who drive the Serial Flash: Southbridge, Super I/O, Embedded Controller, and MCU (Microcontroller), etc.

II. Board Design Note

1. Whether In-system programming (ISP) can be successfully programmed has a lot to do with the circuit design of the board. Please refer to the application file AN0103 to confirm the circuit design of the board: **https://www.DediProg.com/download/save/617.pdf**

2. It is recommended that the length of the cable connecting the programmer and the board should not exceed 10cm, and do not use flying leads.
   Problems with long cables and flying leads:

   (1) Inductive effect: slender cables and wires have a large inductance, which will cause the signal load capacitance to become larger, and the signal may degrade and become worse, resulting in errors.

   (2) Using flying leads, there may be problems of mutual interference of signals.

3. When programmer is programming the Flash on the board, the “Chipset” on the board cannot use SPI Bus at the same time.

4. Chipset has a reset/enable pin; please connect it to the IO3/RESET of the programmer. During programming, IO3/RESET will send a LOW-level signal to make the chipset not work to ensure that it will not interfere with the SPI during programming Signal.

5. SPI outputs are in High Impedance when the Chipset is reset.

6. When board is in Stand By mode (supplied but not turned ON), the chipset and memories are supplied and the chipset release the SPI bus in high Impedance.

7. When board has finished booting, the chipset releases the SPI bus in high Impedance.

8. SPI NOR Flash WP Pin: Write Protect pin, must set to inactive level (to logical H) while programming the SPI NOR Flash.

9. SPI NOR Flash HOLD Pin: Input signal, which is used to pause communication. Must be connected to inactive level (to logical H) while operating with SPI NOR Flash.

10. Selective powering: Can you power the SPI NOR Flash chip without starting the rest of the system? If giving power to that chip means you power the Chipset it's connected to, and you have no way of stopping that Chipset from using the SPI lines you want to connect to talk to the memory chip, then this can't work. In essence, you'll have a hard time if the SPI NOR Flash chip and the Chipset run from the same power supply, and the Chipset does not have an externally accessible reset/enable pin. Also, if the same power supply powers other components, what will happen?

III. In-System Programming (ISP) Solution Reference

1. Please provide the following information to DediProg

1.1 Please provide a complete or partial circuit diagram of the board. Part of the circuit diagram should include:

(1) If the chipset on the board is connected to the SPI NOR Flash, please provide the circuit diagram of the chipset.
(2) Circuit diagram of SPI NOR Flash.
(3) The circuit diagram of the Header on the board.

1.2 Please describe the pin assignment between the DediProg programmer and the SPI NOR Flash on the board.

1.3 Is the chip set on the board circuit isolated to protect the SPI Bus signal of the DediProg programmer from interference?

1.4 Refer to "Updating Methods" on page 12 of the application file AN0103. Which method do you use to update the SPI NOR Flash on the board?

1.5 Which connection method is used between the DediProg programmer and the board? Please describe the connection method and take a photo for our reference.

For example: SF600 → SF600 ISP Cable → SPI NOR Flash on the board

SF600 ISP Cable: **https://www.DediProg.com/product/ISP-600-CB1-G**

1.6 How long is the cable length between the DediProg programmer and the board?

1.7 Is the power supplied by the SPI NOR Flash board or the DediProg programmer?

1.8 Will the chipset on the board work while programming the SPI NOR Flash on the board? If the chipset also works, will the chipset interfere with the SPI Bus signal of the programmer?

1.9 While programming the SPI NOR Flash on the board, is the SPI NOR Flash WP Pin (write protection pin) connected to an invalid level (logic H)?

1.10 While programming the SPI NOR Flash on the board, is the SPI NOR Flash HOLD pin (input signal used to suspend communication) connected to an invalid level (logic H)?

1.11 Does the "Chipset" have a reset/enable pin? If so, please connect this pin to the IO3/RESET Pin of the programmer. During programming, IO3/RESET will send a low-level signal to stop the "Chipset" from working to prevent the "Chipset" from using the SPI Bus at the same time.

1.12 When the "Chipset" is reset, is the SPI output in a high impedance state?

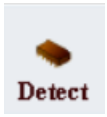
1.13 Does the "Chipset" release the SPI Bus with high impedance after the board is booted?

Please refer to the following steps to troubleshoot the problem first, and send the results to DediProg.

2. Offline programming SPI NOR Flash: check whether the programmer and chip are normal.
   Note: This approach is to clarify whether the chipset on the board will interfere with the programmer's SPI Bus signal output.

   2.1 Desoldering SPI NOR Flash from the board.

   2.2 Connect SPI NOR Flash to DediProg programmer (Please take a photo of the connection method for DediProg reference).

   2.3 Can it Detect 

SPI NOR Flash successfully?

   2.4 Can Program 

and Verify 

work successfully after loading the programming file?

   2.5 If it can detect, program 

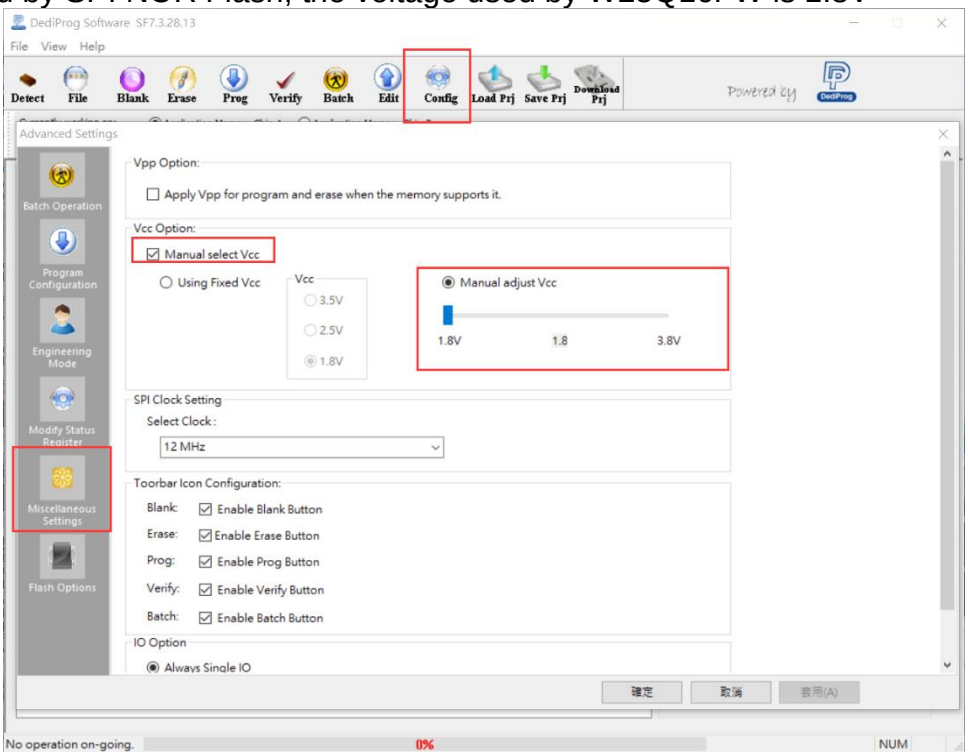
and Verify 

the SPI NOR Flash successfully in offline programming, it means that the software, programmer, and SPI NOR Flash are not having problems.

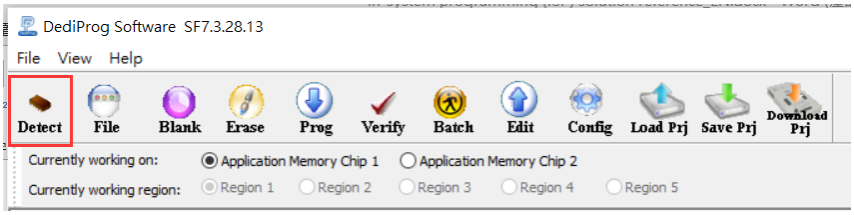
   2.6 Solder the SPI NOR Flash back to the board

3. Use an oscilloscope to measure whether the voltage of the SPI NOR Flash VCC Pin is normal during Detect.
   Note: The following uses Winbond W25Q16FW as a demonstration, the Clock frequency is preset to 12Mhz

3.1 Click the “Config” button→click the “Miscellaneous Setting” button→click the “Manual select Vcc” button→click the “Manual adjust Vcc” button to adjust the voltage supported by SPI NOR Flash, the voltage used by W25Q16FW is 1.8V



3.2 Run Detect



3.3 Observe whether the voltage of the SPI NOR Flash VCC pin is normal when the oscilloscope measures the SPI NOR Flash VCC pin in Detect Chip.

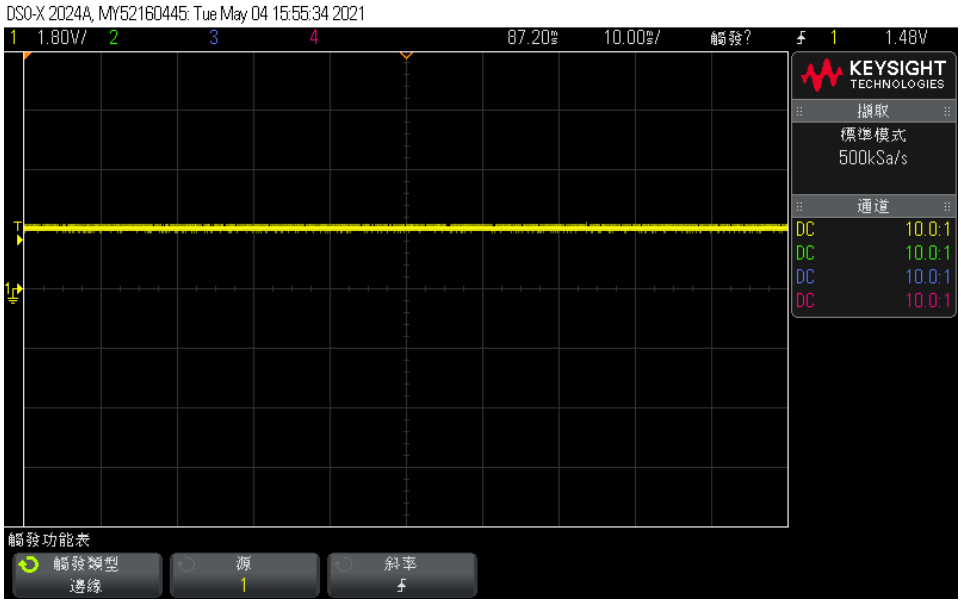
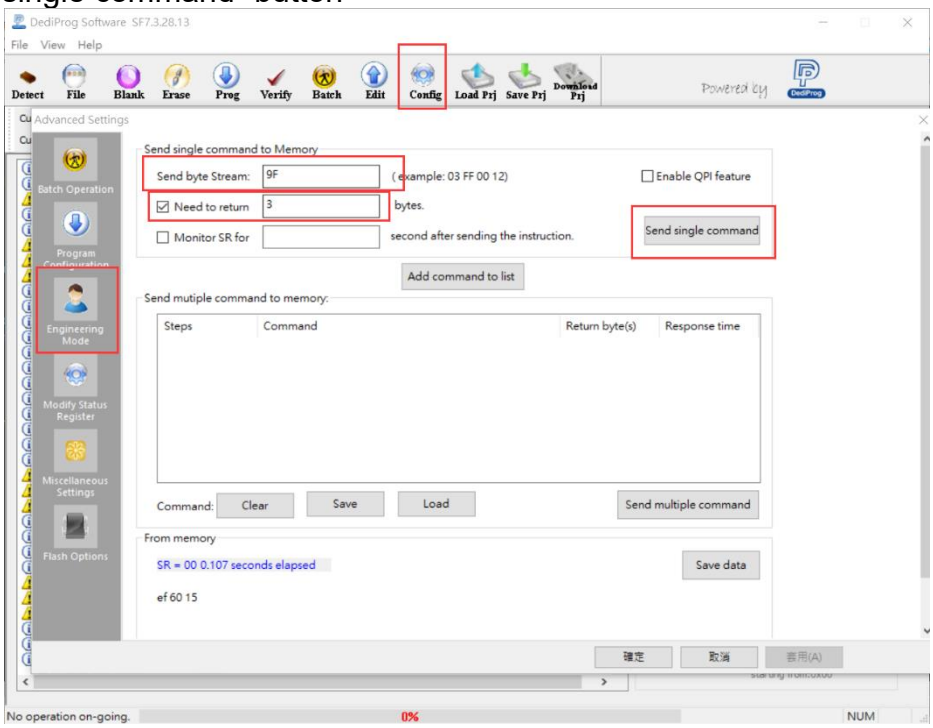


Figure: SPI NOR Flash VCC Pin measured by oscilloscope is 1.8V, and the voltage is normal.

4. Use an oscilloscope to measure whether the waveforms of I/O pins such as SPI NOR Flash CS, CLK, MOSI, and MISO are normal when the Read ID Command (9F) is sent.
Note: The following uses Winbond W25Q16FW as a demonstration, the Clock frequency is preset to 12Mhz

4.1 Click the “Config” button→click the “Engineering Mode” button→Send byte Stream: input Read ID Command(9F) →tick “Need to return” box and fill in the number 3→click the “Send single command” button



4.2 The oscilloscope uses the edge to trigger the rising edge of MOSI to trigger the first MSOI output. Observe the following points:

4.2.1 Does CS have a pull low to 0V?

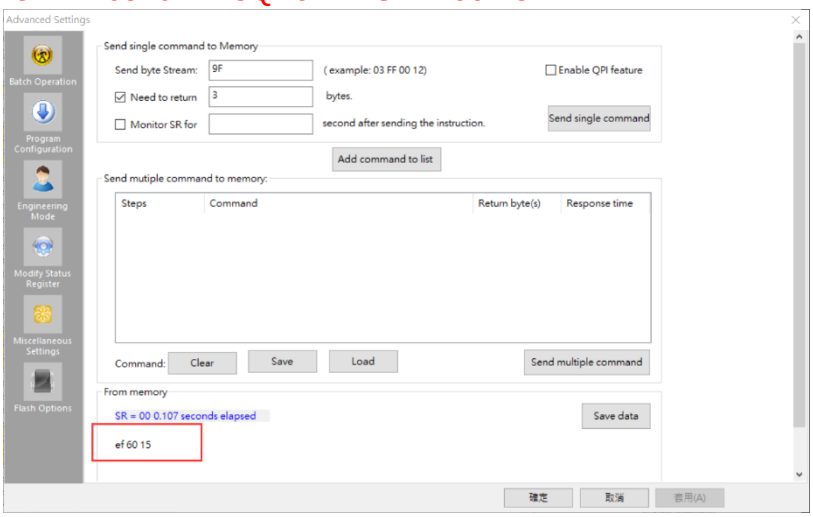
4.2.2 Whether the CLK waveform and voltage are normal?

4.2.3 Is the Read ID Command (9F) waveform output by MOSI correct?

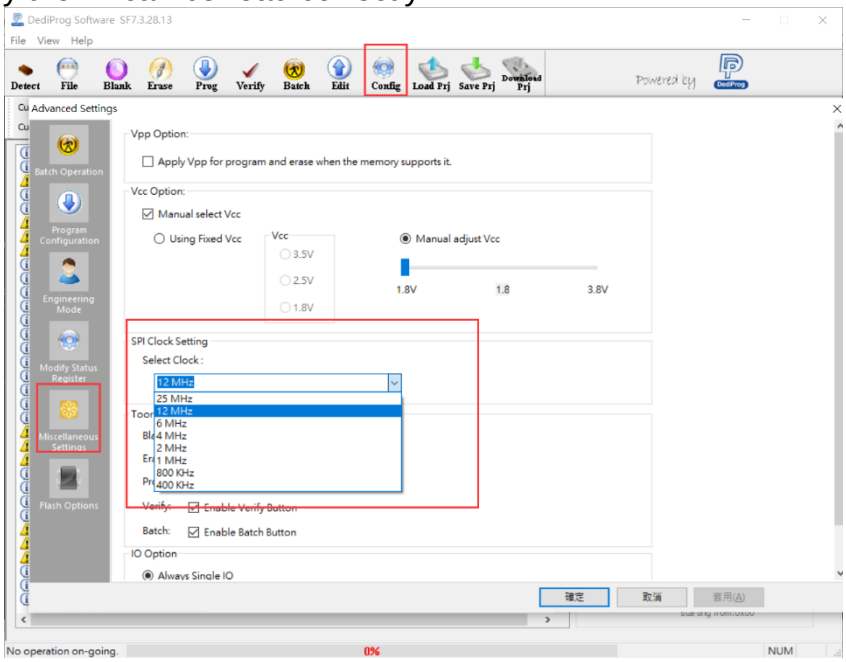
Figure: The Read ID Command of MOSI output measured by the oscilloscope is 9F, and the waveform is correct.

4.2.4 Is the ID returned by the software correct?

Note: The ID of Winbond W25Q16FW is EF 60 15



4.2.5 If the returned ID is incorrect, please lower the frequency in order (12Mhz→6Mhz→4Mhz…→400Khz) and repeat the test above to observe which frequency the ID can be read correctly.



5. If the output voltage is normal, the Detect can also be successful, but the verification fails when batch is executed. Please lower the frequency in order (12Mhz→6Mhz→4Mhz…→400Khz) and repeat the batch again, and observe which frequency for batch can be successfully executed.

IV. Revision History

Date	Version	Description
2021/8/24	1.0	Initial release
2022/5/04	1.1	Added the first chapter "Name Interpretation " Adjusted the text and sequence of steps in Chapter 3 "In-system programming (ISP) Solution Reference"
2022/7/18	1.2	Modified the second description in chapter II.

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